Besi Hybrid Bonding Presentation

December 2021

Safe Harbor Statement

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward-looking statements, which are found in various places throughout the press release, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward looking statements, although not all forward looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward looking statements. While these forward looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 pandemic and measures taken to contain the outbreak, and the associated adverse impacts on the global economy, financial markets, and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region; potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers as a result of the COVID-19 pandemic; those additional risk factors set forth in Besi's annual report for the year ended December 31, 2020 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.

Agenda

- Overview — Richard Blickman, CEO
- Hybrid Bonding Opportunity — Ruurd Boomsma, CTO
- Q&A

Summary

- Semiconductor assembly has moved from individual chip component circuitry to integration on chip level via hybrid bonding. Gating item for semiconductor development
- Hybrid bonding adoption has become most critical element to increasing circuitry speed and further reducing cost
- Has potential to become leading technology for <7nm nodes
- Will coexist with TCB/advanced flip chip and drive growth of high end assembly equipment market
- All leading semiconductor producers evaluating technology
- Market has potential to significantly exceed initial expectations
- Besi has a leading position with competitive advantage

Besi's Hybrid Die Bonding Progress

Status Today

- Initial proof-of-concept orders received in Spring 2021
- Additional orders received in both Q2 and Q3-21 for delivery in H1-22
- Cluster tools available in Q1-22 to help support volume production
- Multiple customer engagements

Capacity/Support Expanded

- Expanded R&D teams in Europe and Singapore
- Completed clean room facility Austria (Q1)
- Added clean room production facility Malaysia (Q4)
- Building capacity to produce 12-15 systems per month
- Engineers and software developers hired for US and Taiwan support

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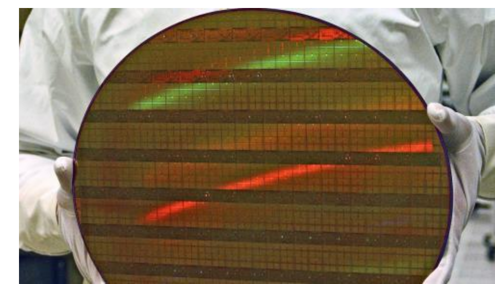
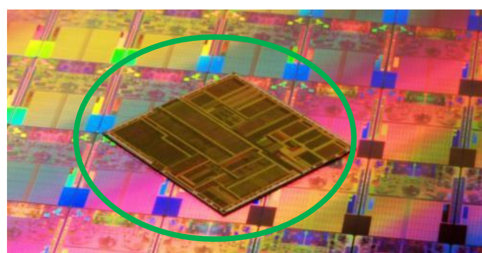
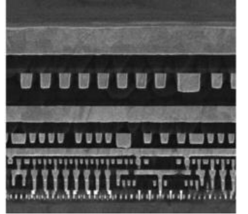
Semiconductor Value Chain

FRONT-END

CREATING ELECTRONIC DEVICE ON SILICON WAFER FROM SIMPLE DIODE TO HIGHLY COMPLEX ICs





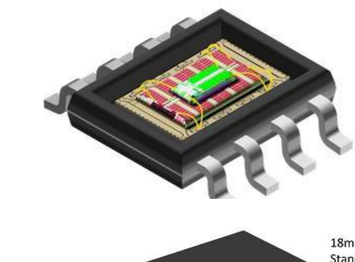


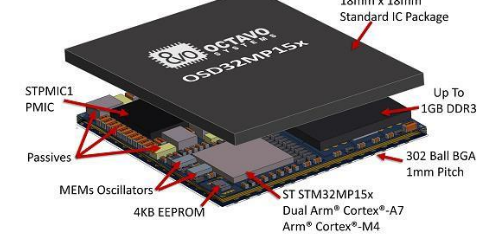
Source: Intel, Anandtech

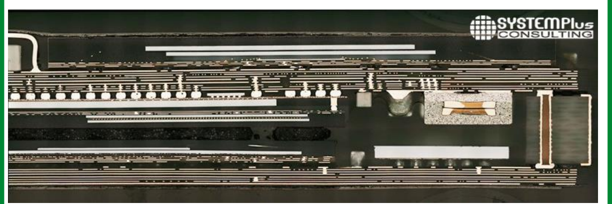
nanometers

ASSEMBLY (BACK-END)

EQUIPMENT TO
PLACE DIES ON CARRIER
CONNECT TO OUTSIDE WORLD
PROTECTING THE DIE
COMBINING DIES IN PACKAGE



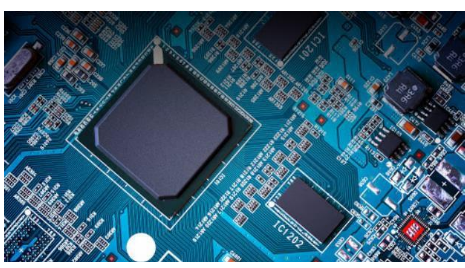




Source: Embedded, ST, System plus consulting

PCB

MOUNTING COMPONENTS
CONNECTING



Source: Techinsight

END PRODUCT

ALMOST ALL PRODUCTS BASED ON OR CONTAIN ELECTRONIC DEVICES

Advanced Packaging Critical to Next Generation Applications

Growth Drivers

Mobile Revolution

- Mobile internet
- Messaging
- Social media
- Shared economy
- Gaming
- Geo-location
- Audio/video
- Auto electronics

Digital Society

- Smart mfg, cities, mobility and homes
- Internet of everything
- 5G mobile/wearable devices
- Artificial intelligence
- Driverless cards
- Data mining
- Cloud servers
- VR/AR
- High performance computing

Enablers

- Greater miniaturization
- Greater complexity
- Increased density
- Higher performance
- Lower power consumption
- Higher accuracy

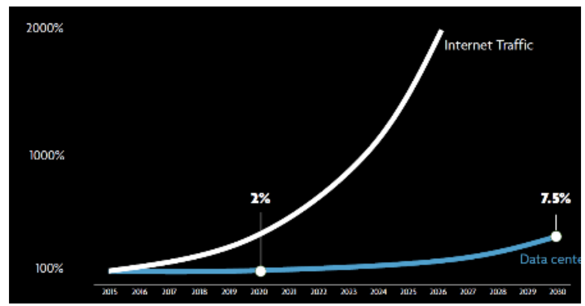
Besi

Die Bonding and Packaging portfolio

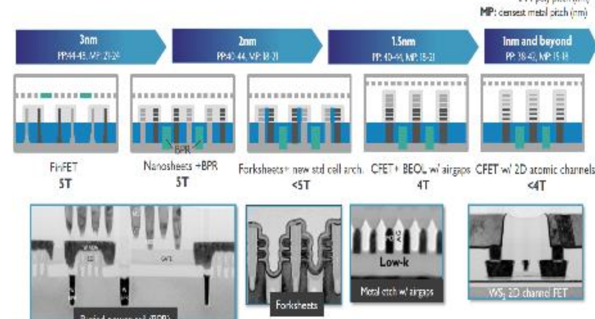
Growth in Advanced Packaging Will Continue as Gateway to Realizing Improved Performance in Next Gen Applications

Advancements in Miniaturization

SMALLER DEVICES ARE FASTER AND REQUIRE LESS ENERGY PER SWITCHING ACTION

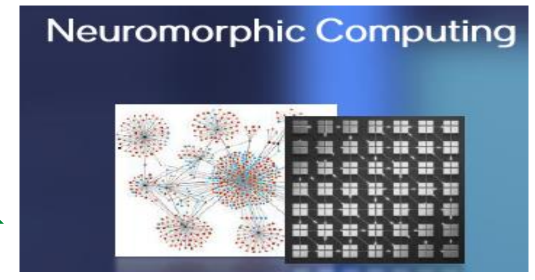


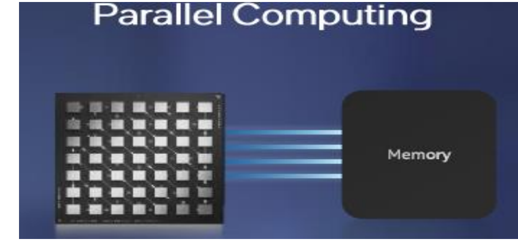
TECHNOLOGY ROADMAPS AVAILABLE



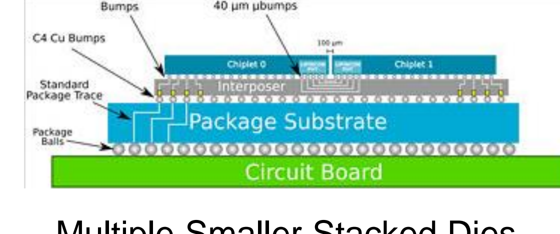
Source: IMEC

New Computing Methods

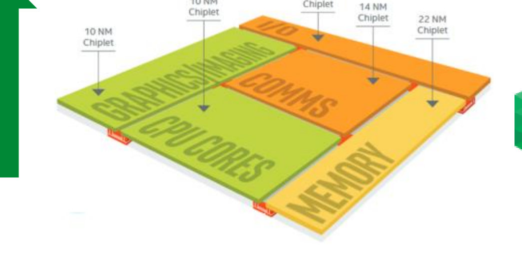




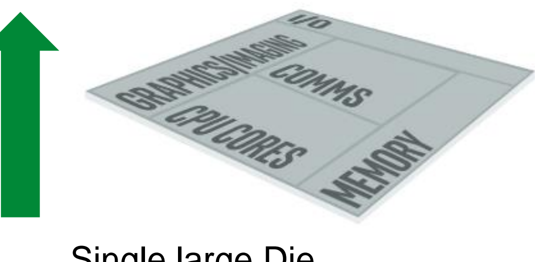
New Packaging Methods: Chiplets / 2.5 D Stacking



Multiple Smaller Stacked Dies

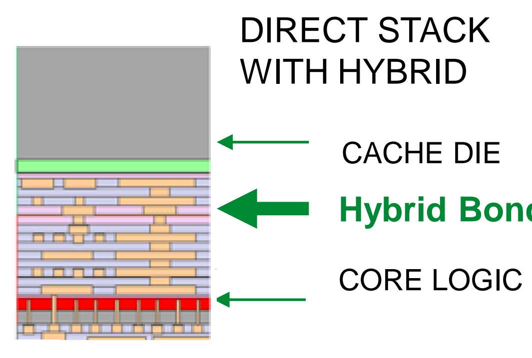


Multiple Smaller Dies
Need more die attach process steps



Single large Die

Real 3D Device Coupling With Die Stacking



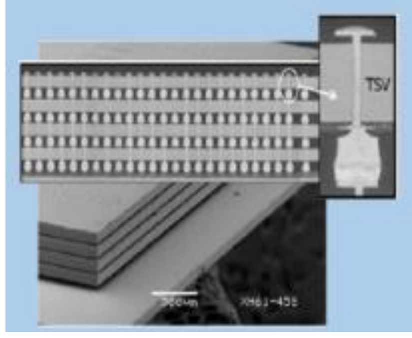
DIRECT STACK WITH HYBRID

CACHE DIE

Hybrid Bond

CORE LOGIC DIE

Besi



3D Stacking with TCB

Extension of Moore’s Law Requires Advanced Packaging Innovation

Moore’s law evolution: the next decade

System scaling to satisfy the need for performance and energy consumption

10^{20}
10^{18}
10^{16}
10^{14}
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
1

1970 1980 1990 2000 2010 2020 2030 2040

System improvements dominated by Transistor scaling ←

System scaling →

Besi

3x/2yrs

4x/2yrs

From transistor to system scaling

Device and layout optimization

System Energy Efficient Performance[3] [1/J·s]

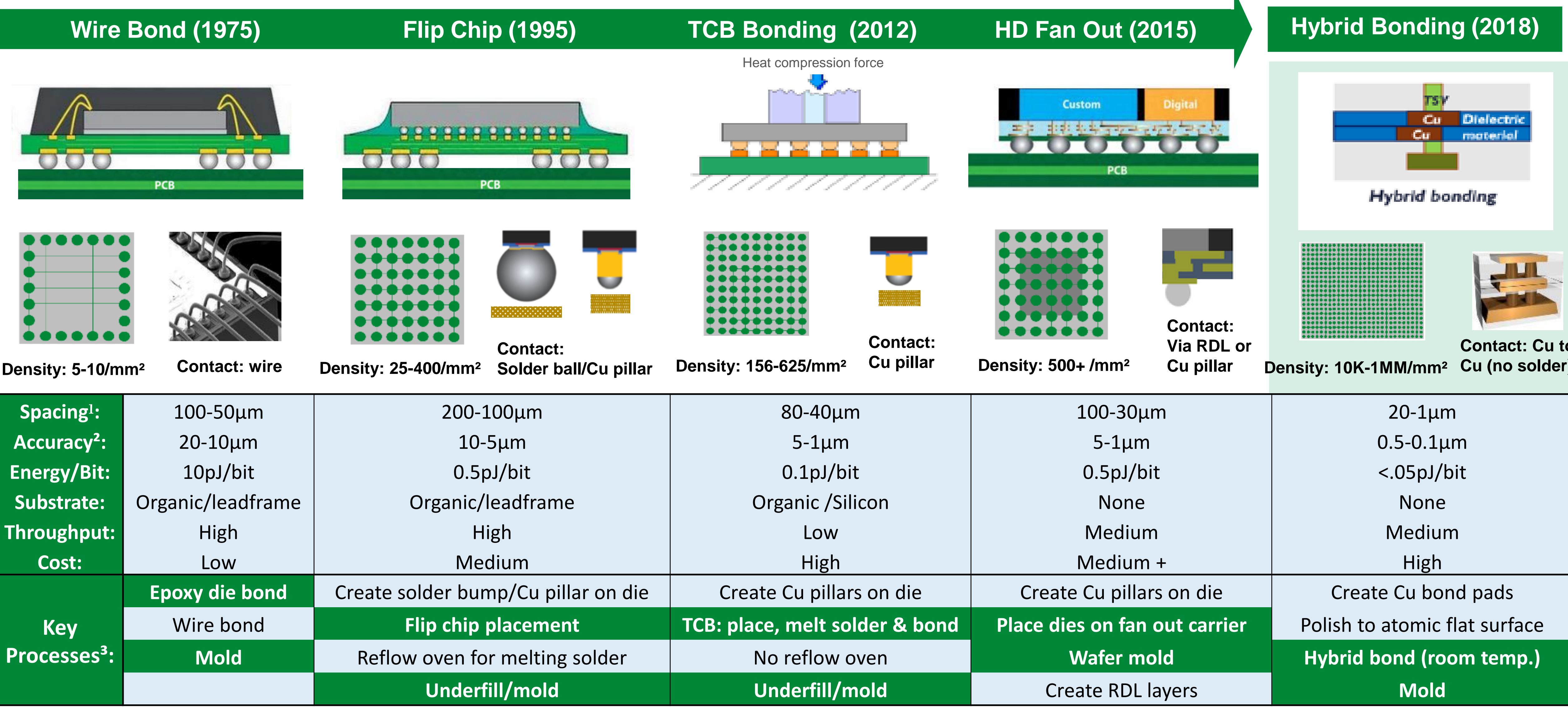
Transistor Energy Efficient Performance[2] [[1/J·s]

Transistor density[2] [#/mm^2]

Litho density[2] (Contact Poly Pitch*Metal Pitch)$^{-1}$ [10^9/mm^2]

Clock Frequency[1] [MHz]

Hybrid Die Bonding: Next Generation Bonding Technology

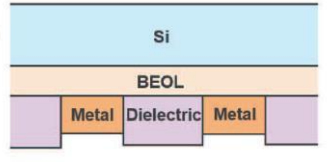


	Wire Bond (1975)	Flip Chip (1995)	TCB Bonding (2012)	HD Fan Out (2015)	Hybrid Bonding (2018)
Spacing[1]:	100-50µm	200-100µm	80-40µm	100-30µm	20-1µm
Accuracy[2]:	20-10µm	10-5µm	5-1µm	5-1µm	0.5-0.1µm
Energy/Bit:	10pJ/bit	0.5pJ/bit	0.1pJ/bit	0.5pJ/bit	<.05pJ/bit
Substrate:	Organic/leadframe	Organic/leadframe	Organic /Silicon	None	None
Throughput:	High	High	Low	Medium	Medium
Cost:	Low	Medium	High	Medium +	High
Key Processes[3]:	**Epoxy die bond**	Create solder bump/Cu pillar on die	Create Cu pillars on die	Create Cu pillars on die	Create Cu bond pads
	Wire bond	**Flip chip placement**	**TCB: place, melt solder & bond**	**Place dies on fan out carrier**	Polish to atomic flat surface
	Mold	Reflow oven for melting solder	No reflow oven	**Wafer mold**	**Hybrid bond (room temp.)**
		Underfill/mold	**Underfill/mold**	Create RDL layers	**Mold**

[1] Contact Spacing. [2] Die Placement Accuracy. [3] Shading denotes Besi process.

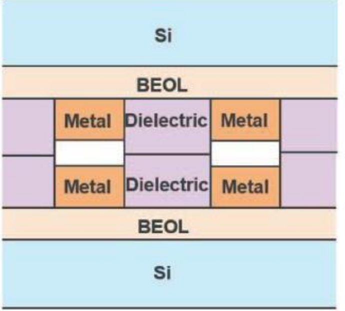
Densities typical for 8x8 mm die size

Understanding Hybrid Bonding

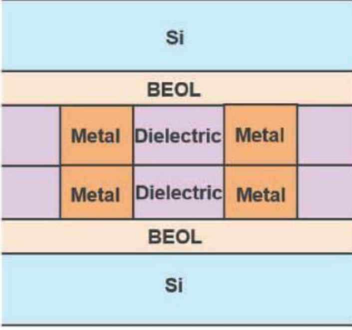


(Plasma-activated surfaces)

1 Preparation
- CMP Polishing
- Very flat < 5nm and clean
- Surface Activation
- Very Clean



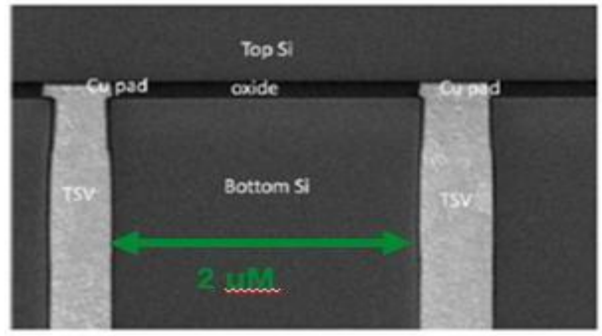
2 Bonding
- Accurate Placement
- Cold Bond
- Based on initial dielectric bond



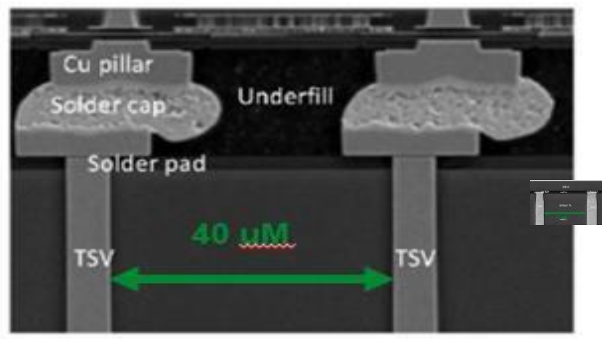
3 Cu-Cu Bonding via Anneal
- Copper expands and contact is made
- Depends on dishing
- Depends on Cu properties

Die to Wafer and Die to Die Bonding of Chiplets

DIRECT CU-CU BOND

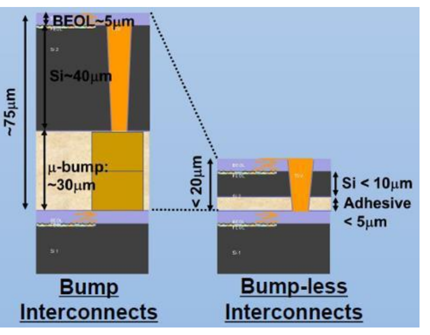


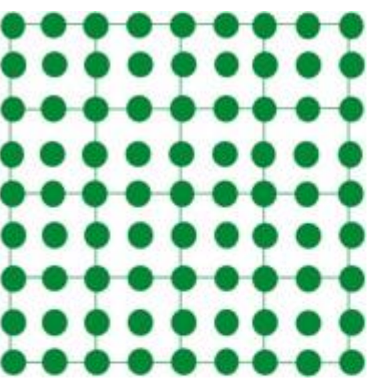
Compare to TCB



Source: XPERI ECTC 2019

BUMPLESS INTERCONNECT





Used below 10 μM Pitch
and contact ! < 200nM Accurate

Merges Front-End/Back-End Processes

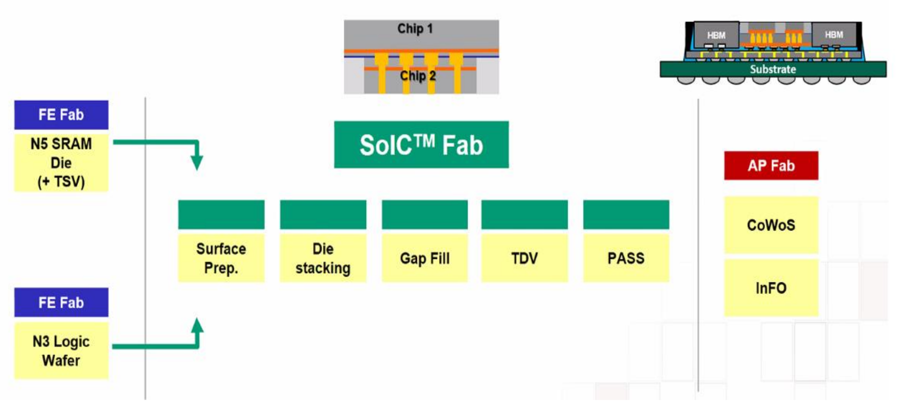
Requiring Much Smaller Dimensions

Reducing cost/contact

C4 (Flip-Chip) ~120/mm² → μ-bump (3DIC) ~ 800/mm² → Bump-less (SoIC) 12,000→ 1,200,000/mm²

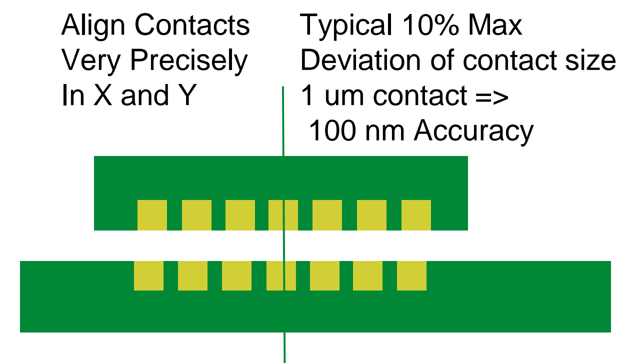
UBM, PI, Pass2, Pass1, AP, Mtop, SI, Cu pillar, HB, Bond dielectric

Hybrid die to wafer bonding much like front-end fab

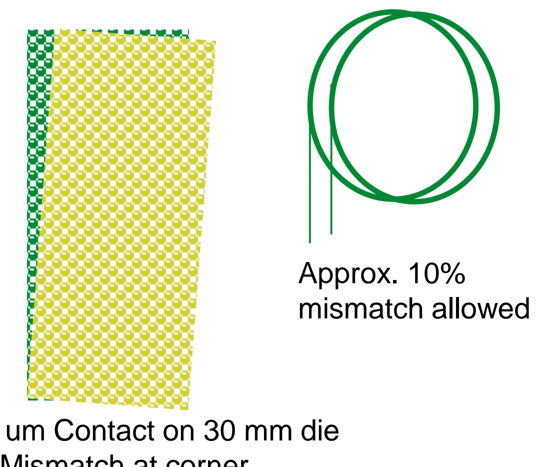


Source: TSMC

Requiring Much Higher Precision



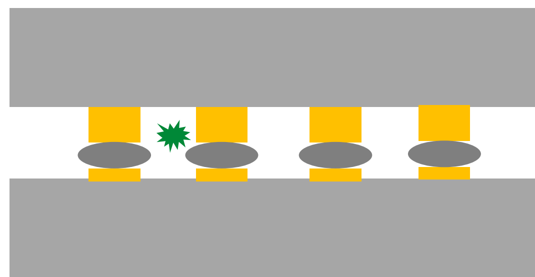
As well as angular control



1 um Contact on 30 mm die
10% Mismatch at corner
3 mm on 1 km

Requiring Higher Levels of Cleanliness Comparable to Front-End Which Drives Upwards ASP

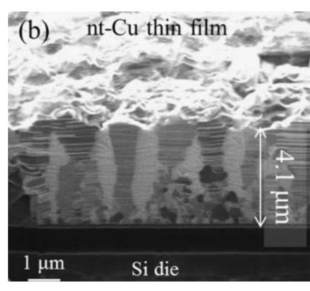
In TCB process, a small particle may have little effect



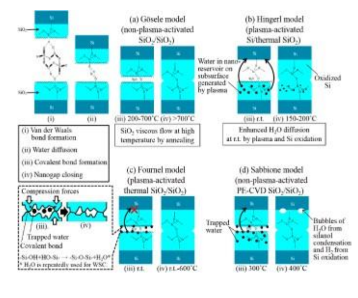
In hybrid process, a small particle may cause an open contact

Many Front-End and Assembly Process Steps Involved in Clean Room Environment

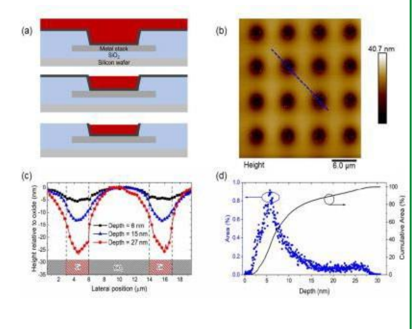
Copper quality and fill



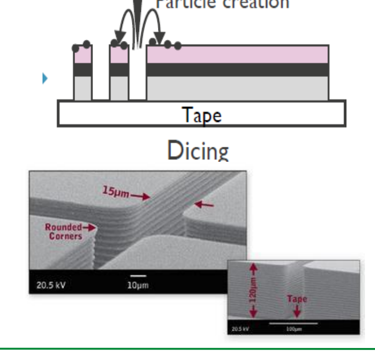
Impact of oxide depostion



CMP and Dishing

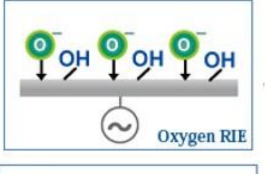


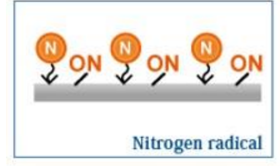
Dicing Cleanliness



Cleaning Parameters

Plasma Activation Parameters





Optimized Bonding Geometry

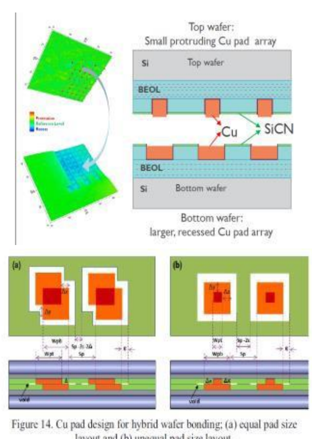
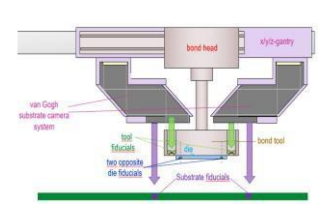


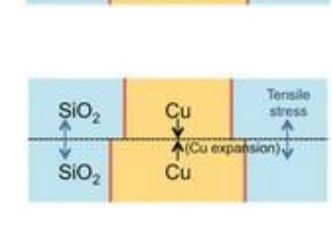
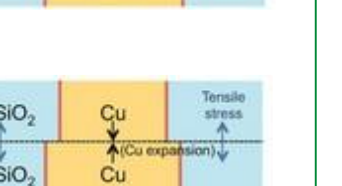
Figure 14. Cu pad design for hybrid wafer bonding: (a) equal pad size layout and (b) unequal pad size layout.

Bonding Process Industrial Solution

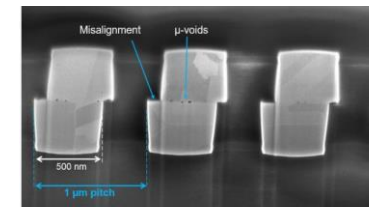


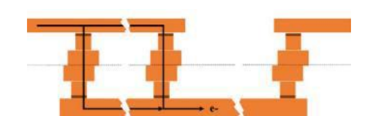
Integrated Process Flow Low Particles Inspection

Anneal

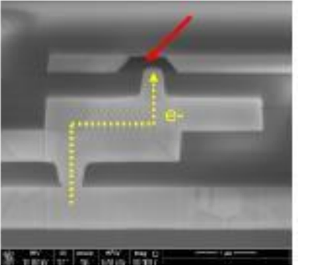
Electrical





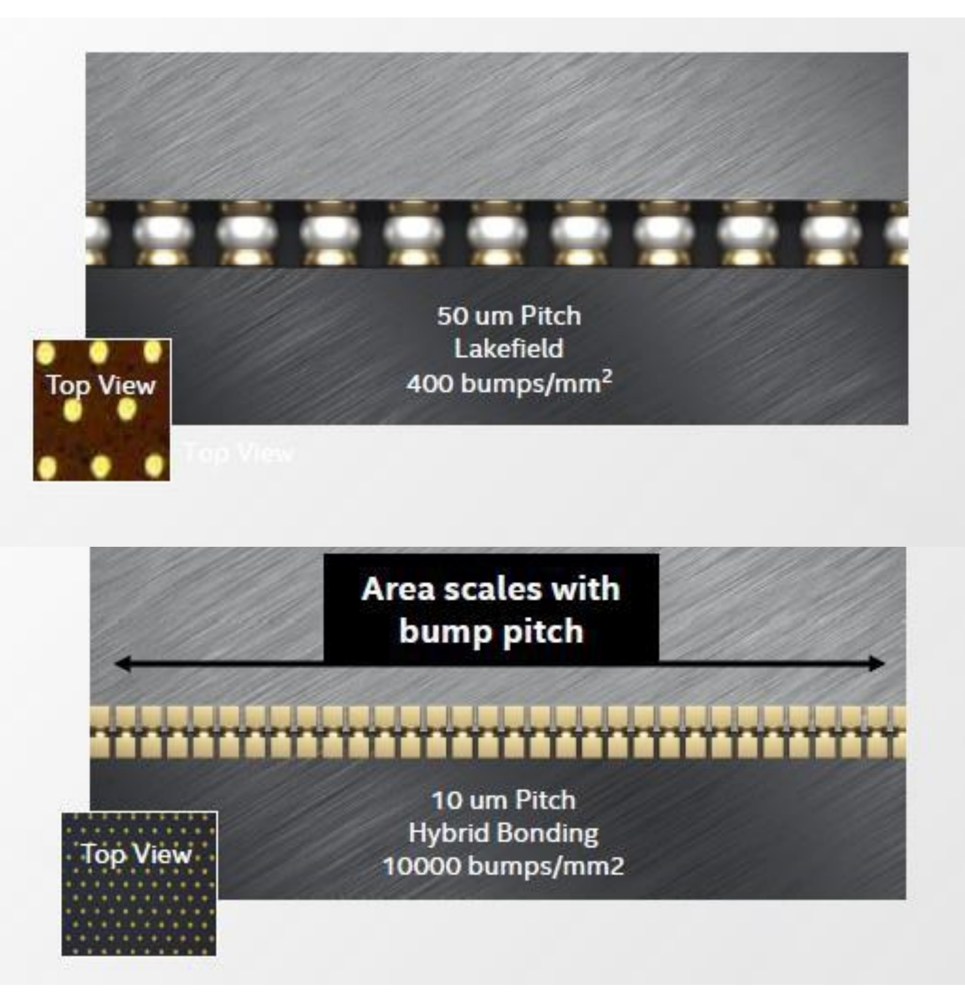
Life Time

- Corrosion
- Electromigration
- Thermal Stability



Hybrid Bonding is a Game Changer for Increasing Contact Density

MORE DATA =>MORE CONTACTS



Source: Intel

Contacts Per mm2

Contact Density at Different Contact Pitches

1'000'000
100'000
10'000
1'000
100
10
1

0 20 40 60 80 100

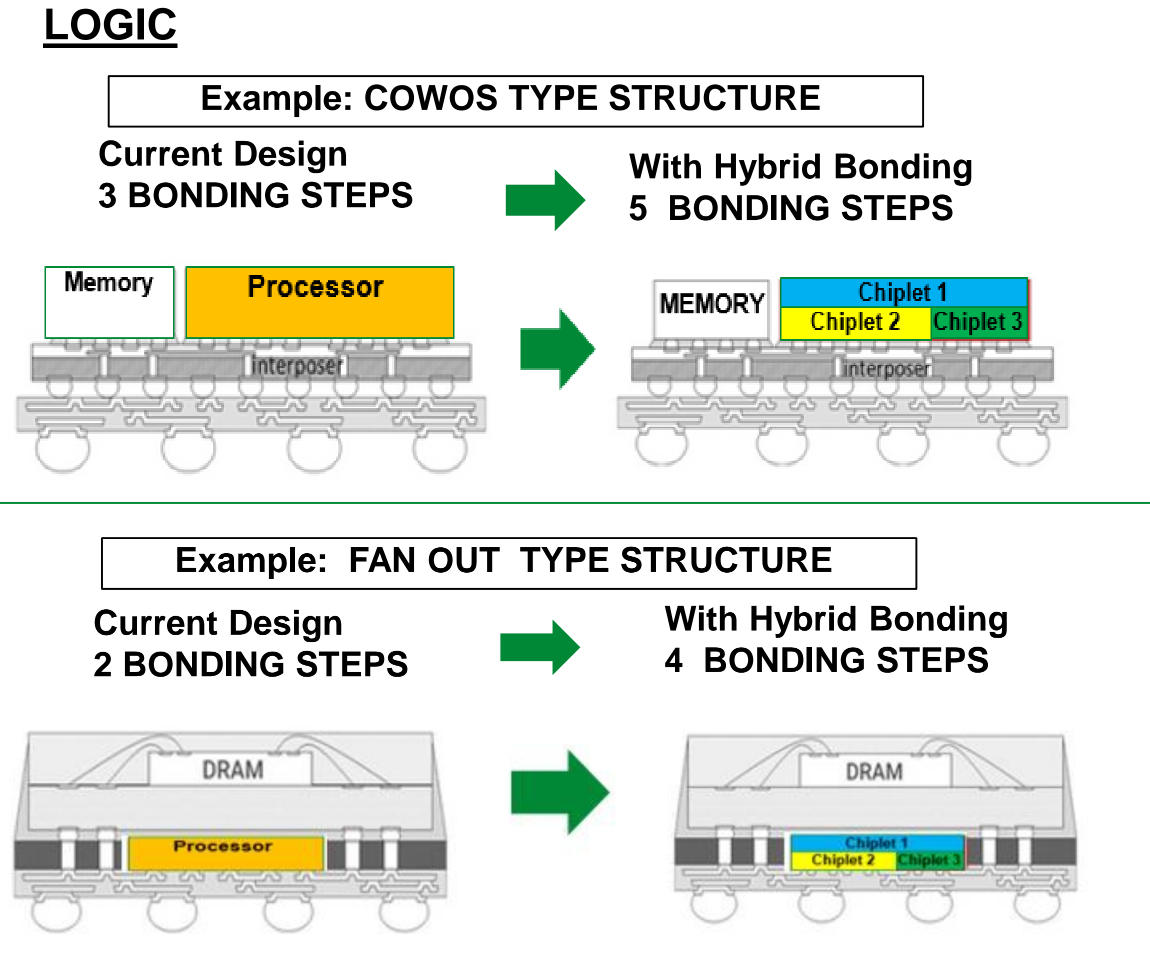
Pitch in um

Hybrid Bumpless
TCB uBump
Flip Chip C4

Bump-less (SoIC)
12,000→ 1,200,000/mm²
μ-bump (3DIC)
~ 800/mm²
C4 (Flip-Chip)
~120/mm²

Requires More Process Steps Resulting in Higher Assembly Capital Intensity

Hybrid Bonding Adoption Will Generate Additional Demand For Assembly Equipment



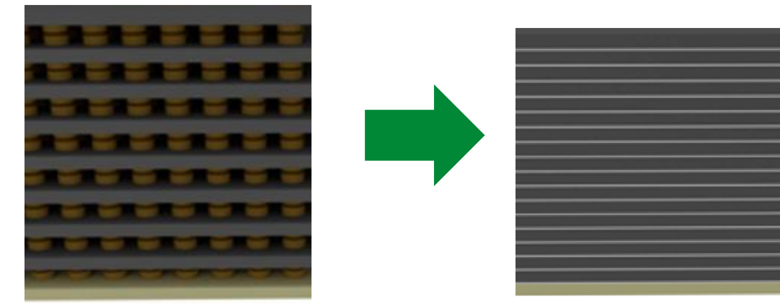
Source: TSMC

MEMORY

CASE 1 => HYBRID MAY REPLACE 1 TO 1 TCB

TCB BONDED HBM — HYBRID BONDED HBM

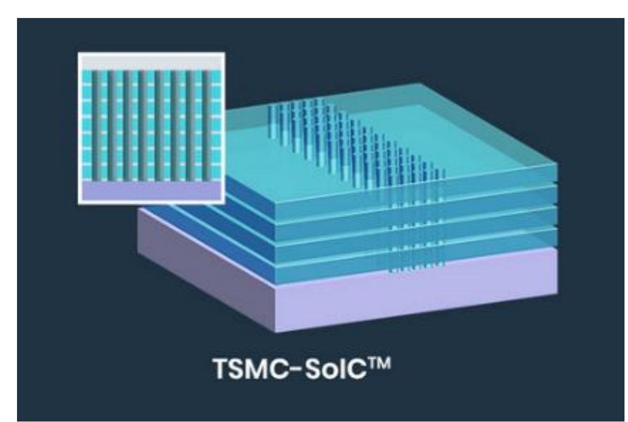
CASE 2 => HYBRID WILL ALLOW FOR MORE DIES IN SAME STACK HEIGHT LEADING TO MORE BONDING STEPS

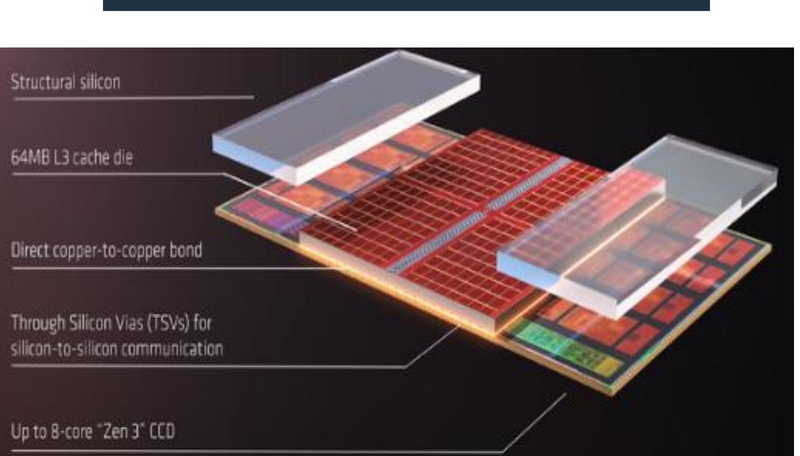


Source: Xperi

Now on Agenda of All Big Players

SAMSUNG





Source: TSMC, AMD presentations

Hybrid Bonding

Enabling new architectures

TSV/Hybrid Bonding

Stacked SRAM

Source: Intel Archtecture Day 2020

Cu Hybrid Bonding Technology

Bonding performance affects package performance *Electrical & thermal

uBump — CoW, Chip on Wafer

Cu-Cu bonding — Bumpless

Bandwidth	Bond Pitch	Allowable Power	Bond Gap
Up to 300% vs CoW	Up to 85% vs CoW	Up to 33% vs CoW	Up to 67% vs CoW

(source : IWLPC 2019, SAMSUNG)

Fine pitch requires continuously New Bump & Bonding Technology

C4 Bump (Flipchip) ~90um pitch ⋙ µ-Bump (2.5D/3D) ~20um ⋙ Bump-less (2.5D/3D) ≤ 10um

(source : SAFE 2020, SAMSUNG)

Source: Samsung presentations

Chiplet Based System With Hybrid Connections is Next Step

AMD 3D chiplet gives an 3.1-3.8 EEP improvement

By integrating memory with the processor in one package

3x power reduction,
4-25% speed improvement

Structural silicon

64MB L3 cache die

Direct copper-to-copper bond

Through Silicon Vias (TSVs) for silicon-to-silicon communication

Up to 8-core “Zen 3” CCD

Source: Lisa Su, AMD, “Accelerating the ecosystem”, Computex keynote 2021, June 2 2021

AMD

AMD EPYC Milan X

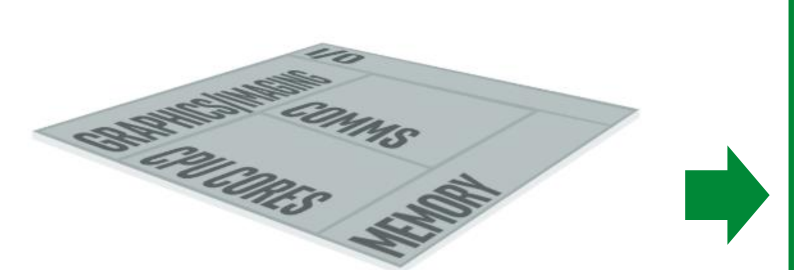
Announced November 2021
Eight CCD chiplets + I/O die
3D V-Cache using hybrid bonding

Chiplet Adoption Enables Cost Effective Means of Increasing Performance

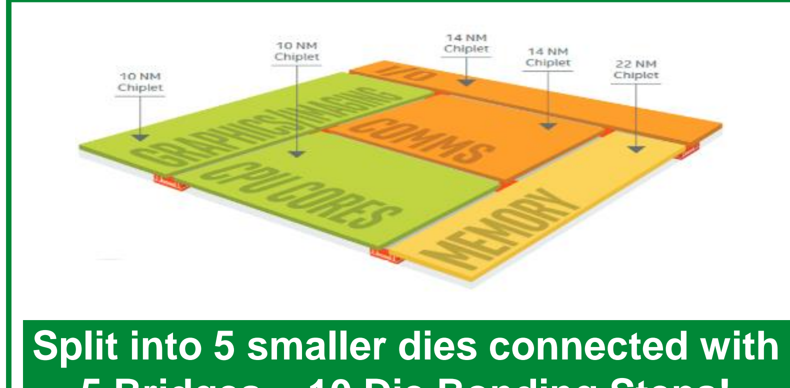
For many years the most direct way to improve capacity and performance was to increase wafer size and design by using smaller devices with more transistors/mm^2

5 nm node seems to be the turning point where chiplet technology becomes more cost effective to further increase performance

Chiplet Adoption Also Increases Assembly Capital Intensity



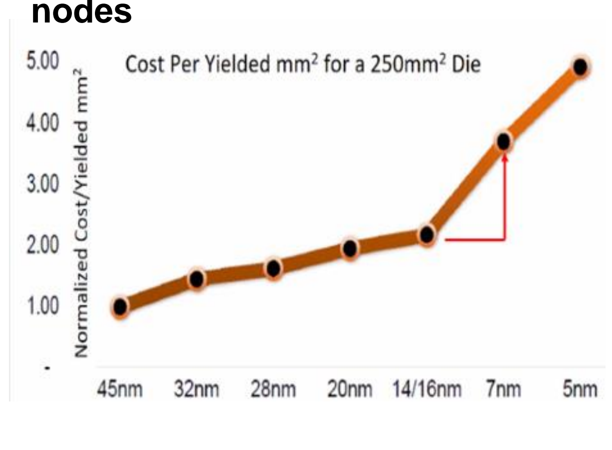
Single Silicon Die
1 Die Bonding Step



Split into 5 smaller dies connected with 5 Bridges = 10 Die Bonding Steps!

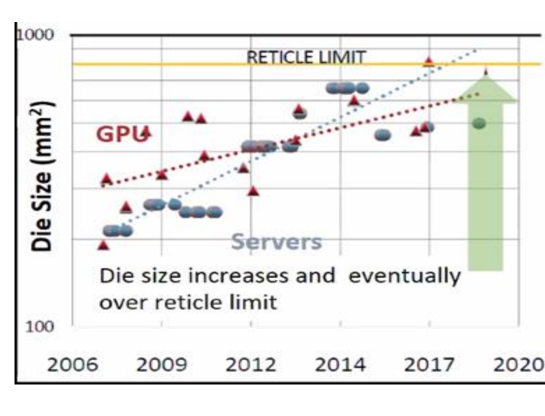
Current Technology Limitations

Investment and design cost per/mm^2 increasing for advanced nodes



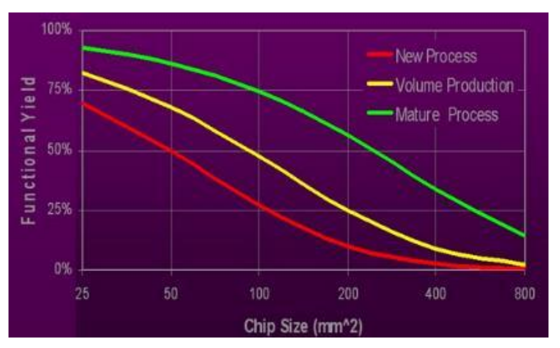
Source: AMD

Size limited by lithography constraints



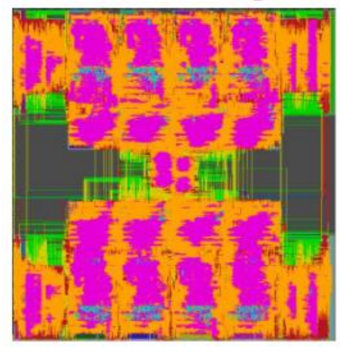
Source: AMD

Usage of larger chips results in lower yields



Source: Toshiba

Wire length between sections can become too long



Source: IMEC

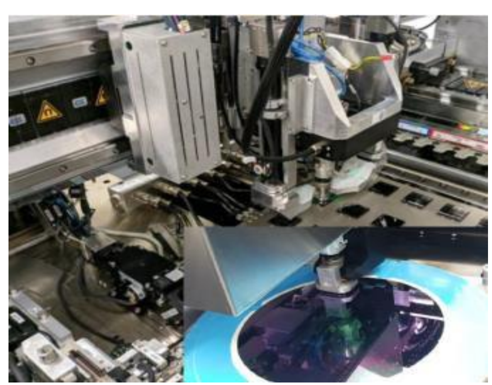
Hybrid Bonding Adoption Leads to Higher Capital Intensity per UPH

8800 FC Quantum
3 micron accuracy

ASP: $500k

~9,000uph

8800 Ultra Accurate Chip to Wafer Hybrid Bonder
<200 nanometer accuracy



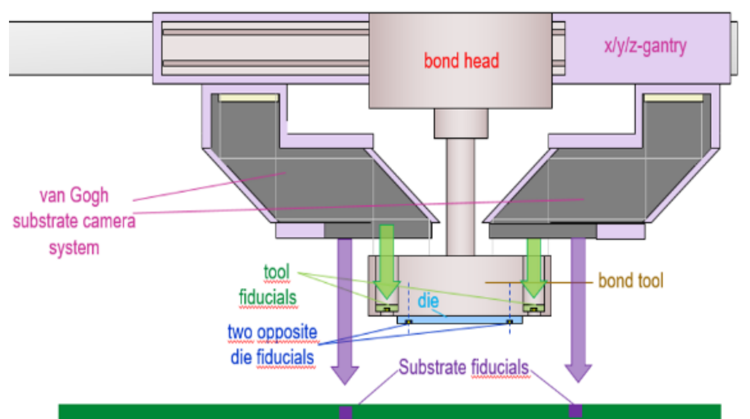
Pricing: $1.5MM-2.5MM
Configuration dependent

~1,500uph

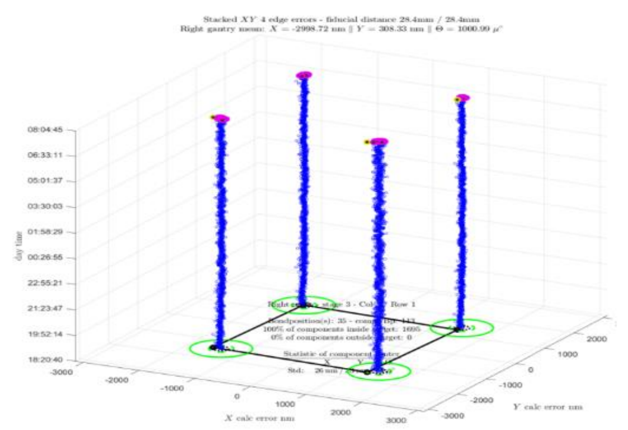
Status Update: Besi/AMAT Development Cooperation

SYSTEM IMPROVEMENTS

REACHING 122nm ACCURACY
OUTPUT UP TO 2,000 UPH



High accuracy placement within 200nm radius



JOINT DEVELOPMENT COOPERATION AMAT AND BESI

ANNOUNCED OCTOBER 2020

- Front and Back-End Process Expertise
- Dedicated Packaging Development Center
- Platform Design and Integration
- Assembly Equipment Process Expertise
- Market Leader in Hybrid Bonding Systems

JOINT HYBRID CENTRE IN SINGAPORE
JOINT DEVELOPMENT OF CLUSTER SOLUTION

SUBSTANTIAL INVESTMENT IN CLEAN ROOM INFRASTRUCTURE, MEASUREMENT EQUIPMENT, AND PEOPLE

Estimated Rollout of Hybrid Bonding Applications

	2022	2023	2024	2025	2026	2027	2028	2029	2030
Computing: Servers/Datacenter/HPC/AI									
Consumer: PC/Laptop/Gaming/Entertainment									
Memory: HBM									
Mobile: High-end smartphone, watch, Airpods									
Automotive: Autonomous driving									
Industrial/Medical									

Hybrid Die Bonding Market Update

HYBRID BONDING EQUIPMENT MARKET

June 2020 estimate

Total # of installed back-end machines for hybrid bonding

Estimated 700-1,400 systems by 2030

1,500
1,000
500
0

2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030

High case
Cumulative Total: € 2.0B

Prediction as per TCB analogy

Low case
Cumulative Total: € 1B

Initial adoption driven by TSMC, followed by Intel and Samsung

Other IDMs and OSATs likely wait until technology matures

Start replacements of initial machines

1 Pre-maturity
2 First entry
3 Confirmation
4 Mass volume / efficiency

Source: Besi estimates

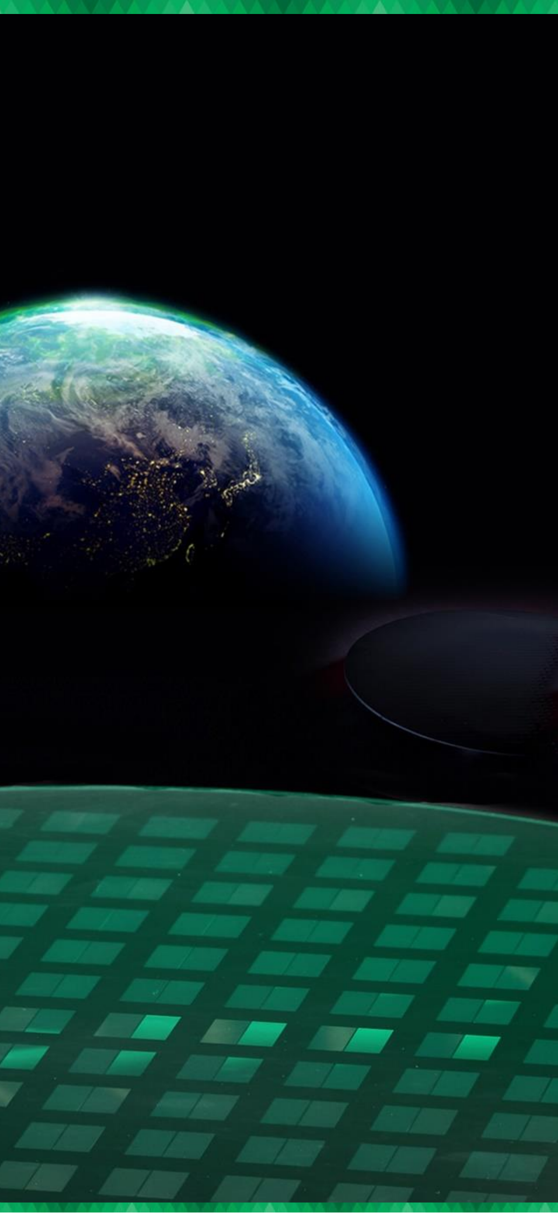
Market tracking above high case developed in June 2020

- High level of customer engagement
- Significant interest expressed by both logic and memory players
- Collaboration with AMAT enhances market position
- AMD first to announce hybrid bonded 3D chiplet-based processor
- Building capacity to € 300-400MM/annum
- **Full adoption by high-end smartphone manufacturers could significantly expand market opportunity**

Forecast highly dependent on timing of:

- Successful design and development per IDM
- Customer roadmaps
- Successful performance in mass production environment

Agenda



▪ Overview	Richard Blickman, CEO
▪ Hybrid Bonding Opportunity	Ruurd Boomsma, CTO
▪ Q&A	